DARPA is building a silicon compiler

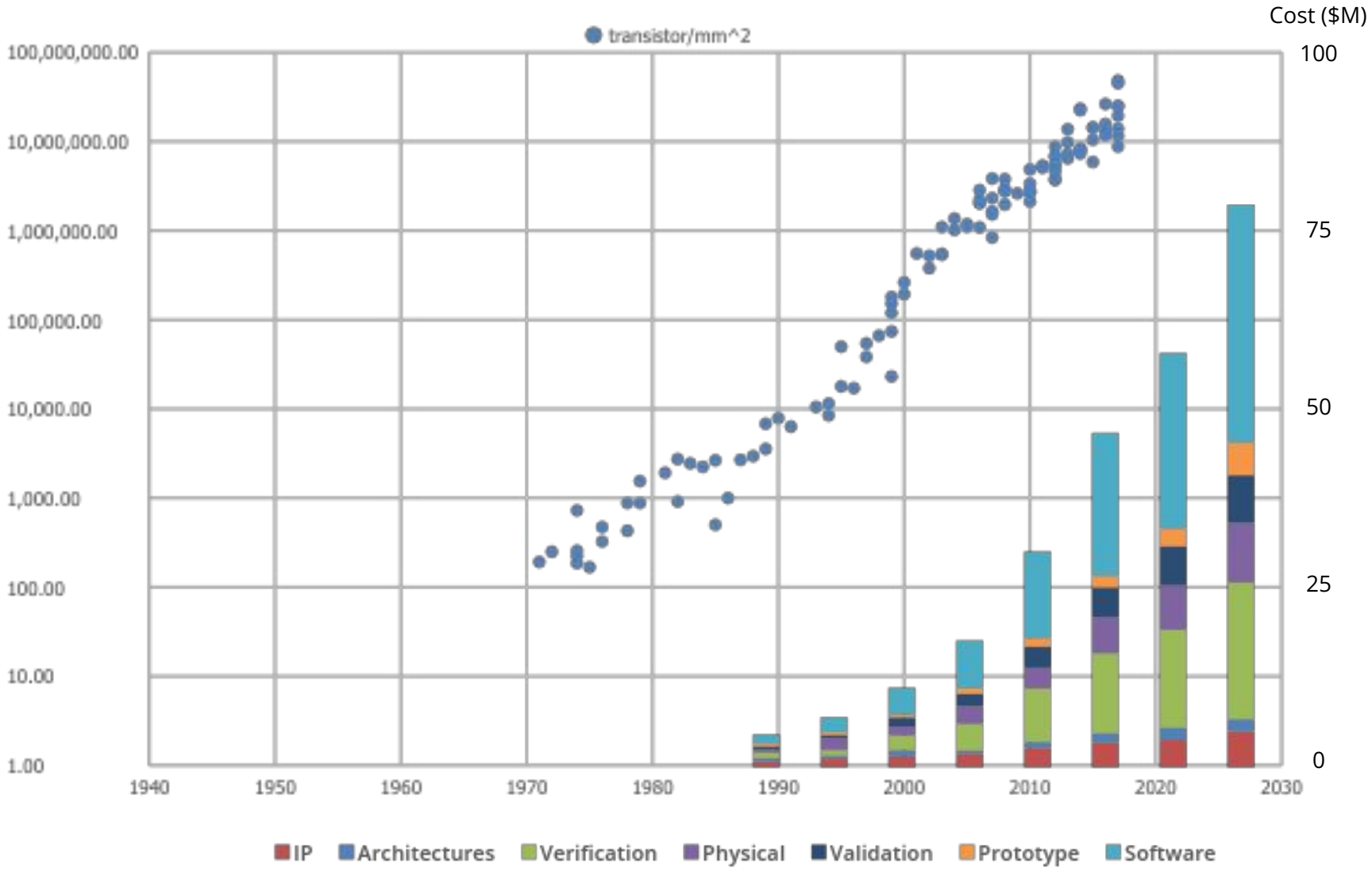
Andreas Olofsson
Program Manager
DARPA/MTO

Design Automation Conference
San Francisco
6/26/2018



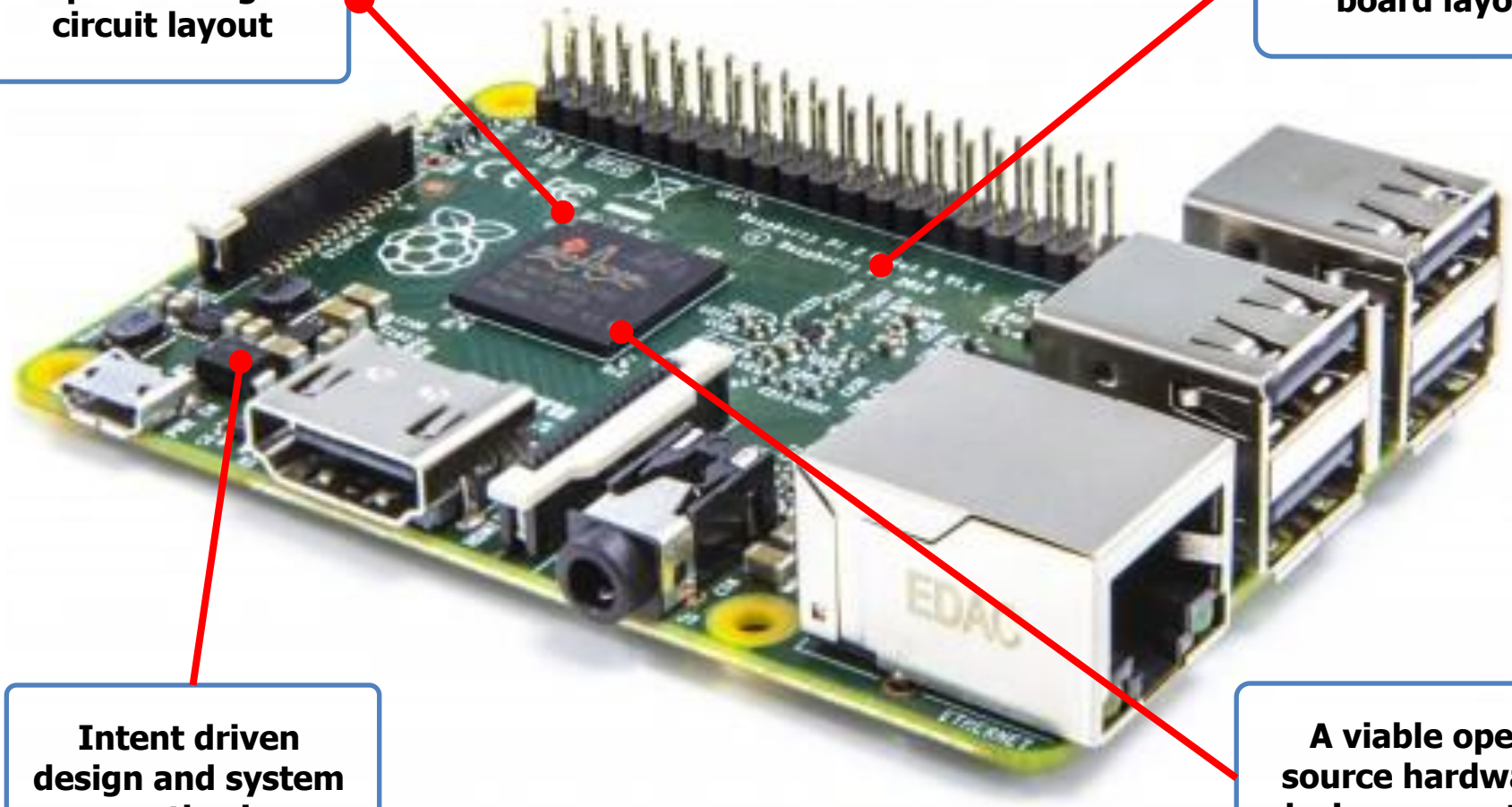
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We are losing the complexity battle



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DARPA's $100M Hardware Compiler Investment



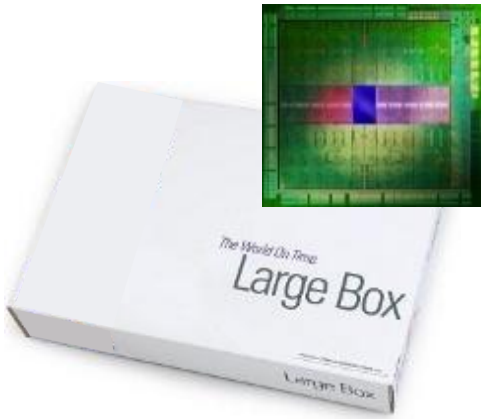
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End State – The first general purpose Silicon Compiler

```
$ git clone https://github.com/darpa/idea
$ git clone https://github.com/darpa/posh
$ cd posh
$ make soc42
```





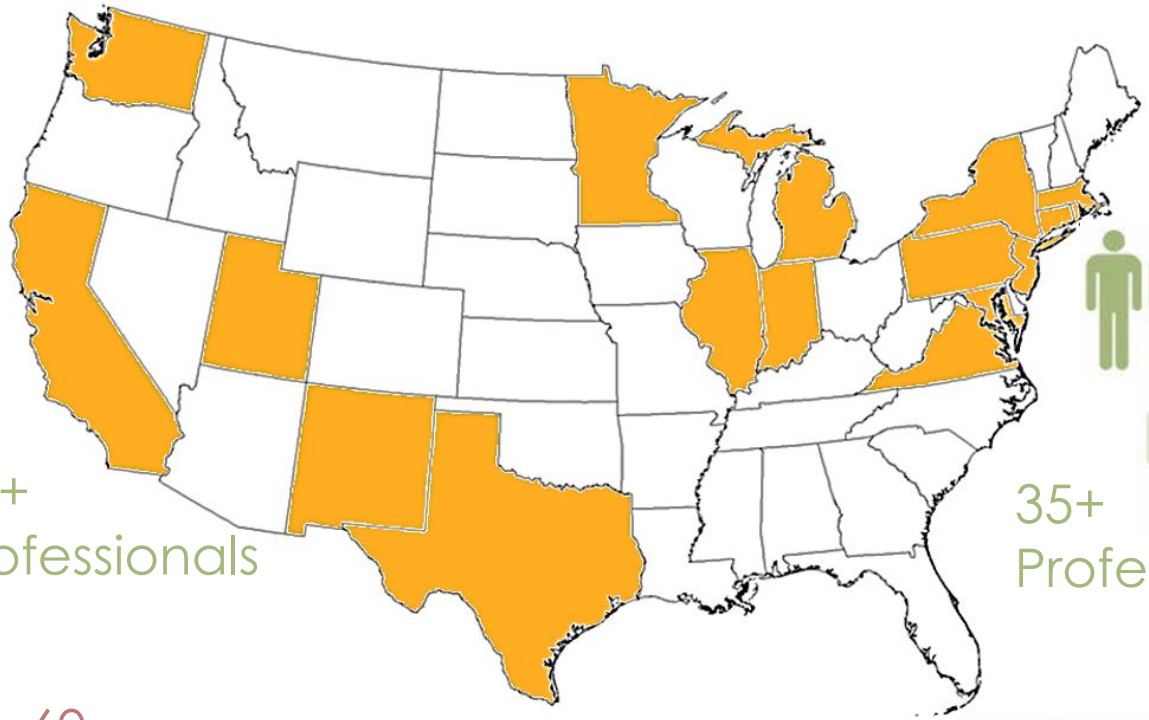


What it takes to build a hardware compiler

IDEA Program
11 Teams
16 Subcontractors

POSH Program
11 Teams
10 Subcontractors

22 Teams Across 17 States



26 Professors

35+ Professionals

18 Professors

35+ Professionals

60 Graduate Students

57% Academic Institutions

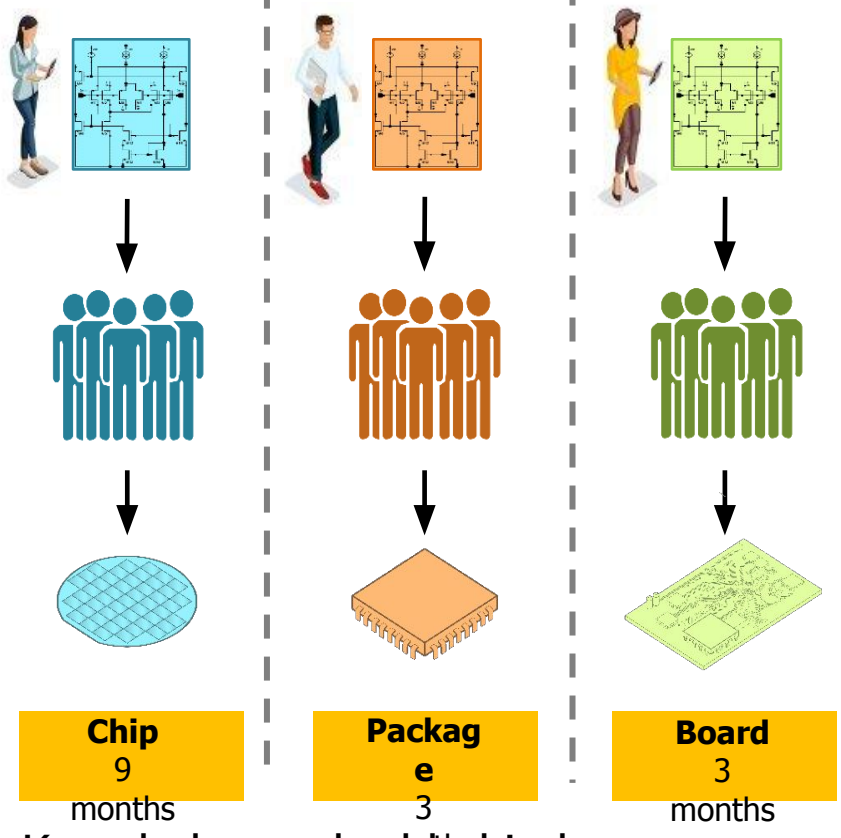
43% Industry

39 Graduate Students

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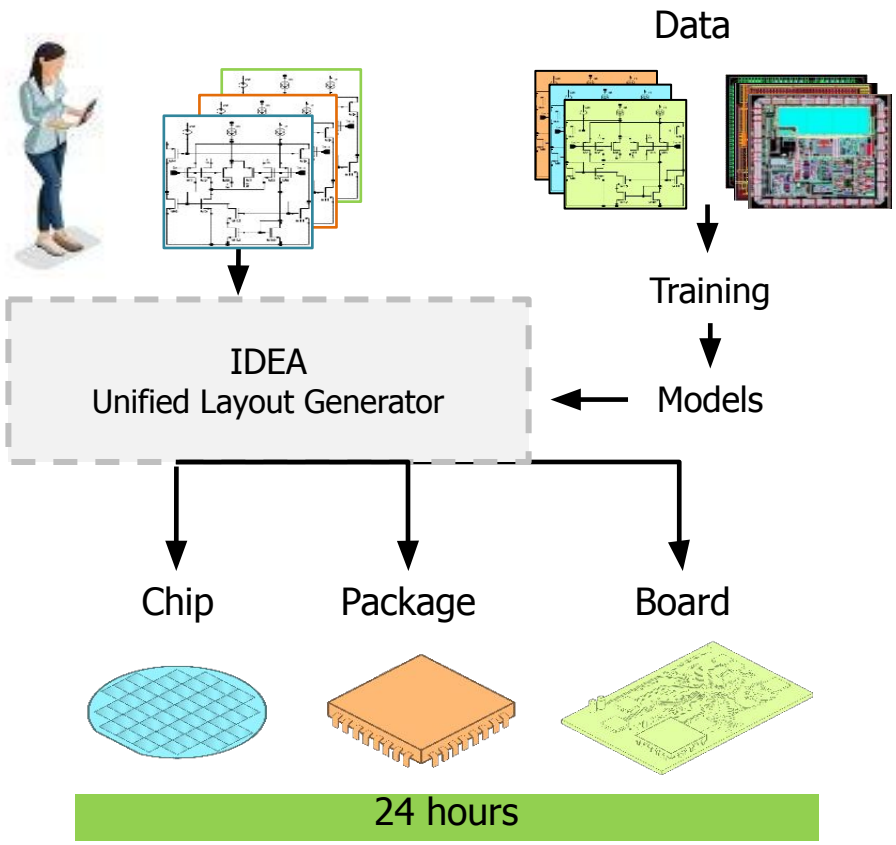
IDEA: A unified electrical circuit layout generator

Today



- Knowledge embedded in humans
- Limited knowledge reuse
- Reliance on scarce resources

Future



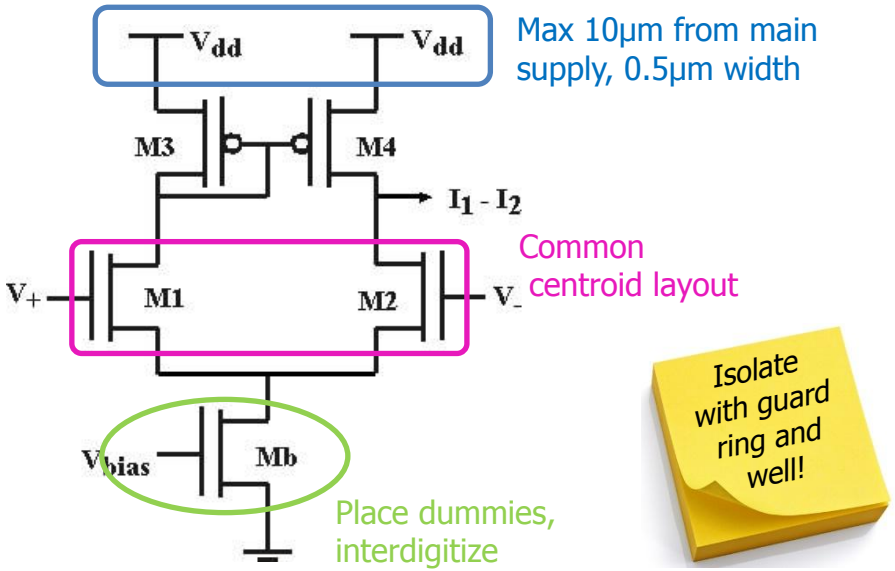
- Knowledge embedded in software
- 100% automated hardware compilation
- 24 hour turnaround

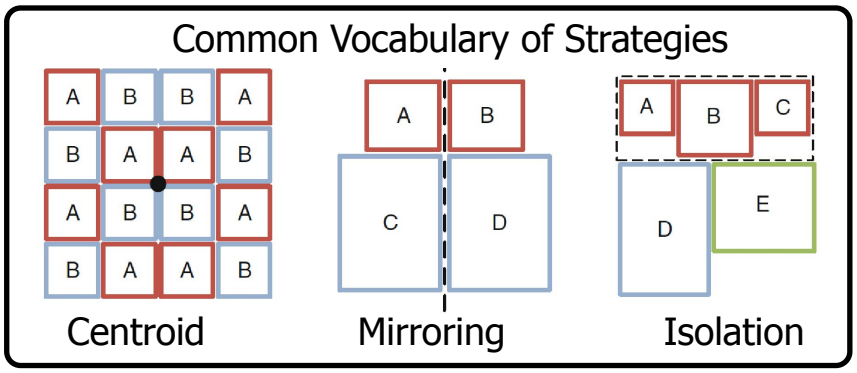
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IDEA: No human in the loop digital AND analog layout!

Today

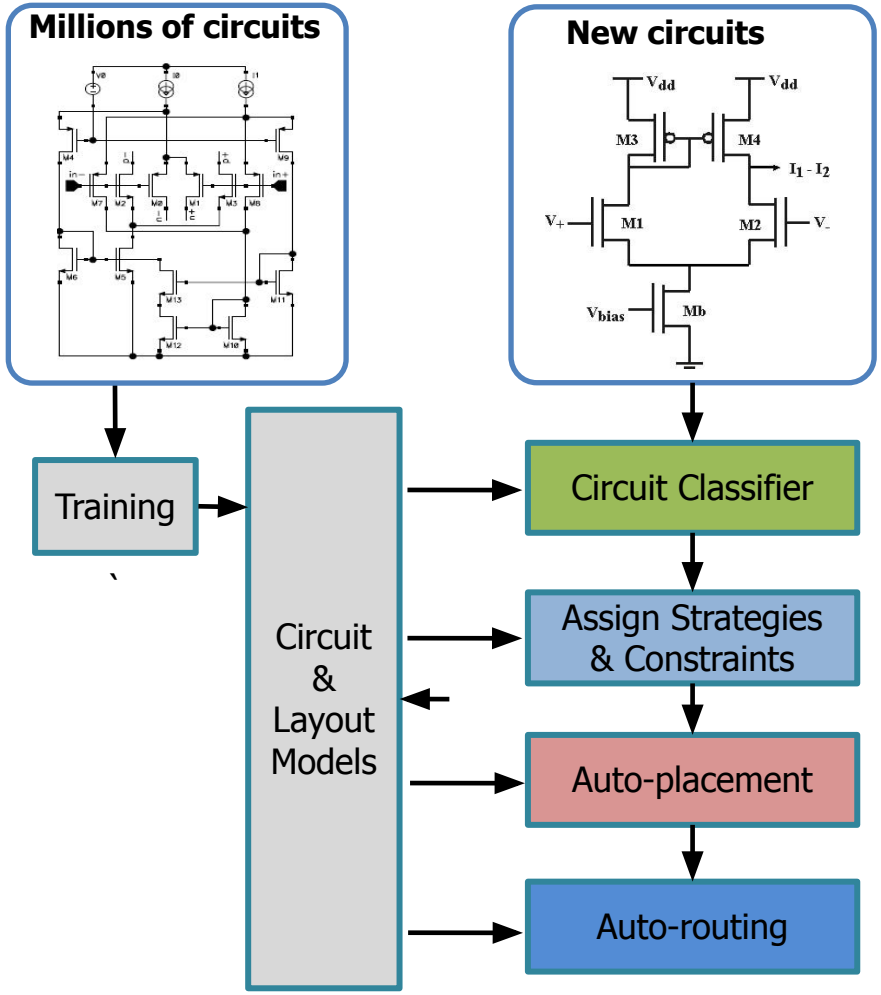
Designer provides manual constraints to layout person (or tool)





Future

Automatically assign constraints based on trained circuit & layout models

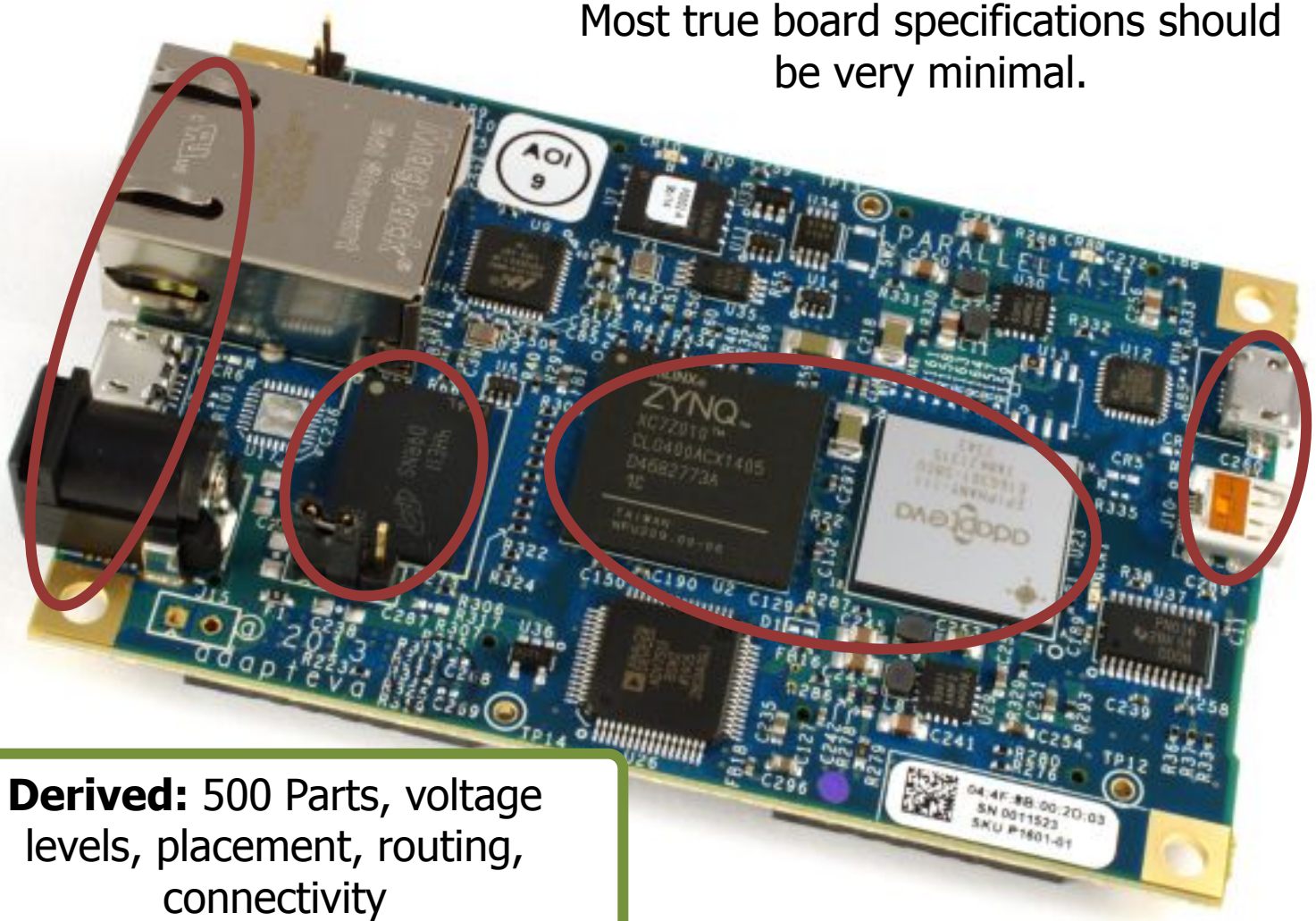


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IDEA: Intent-driven system synthesis

Intent: Specify what, not how!
Most true board specifications should be very minimal.

True Specs:
5V
Ethernet
USB
HDMI
1GB RAM
128MB Flash
FPGPA
20 GFLOPS
ARM A9



Derived: 500 Parts, voltage levels, placement, routing, connectivity

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IDEA: An open 5M+ component IC database

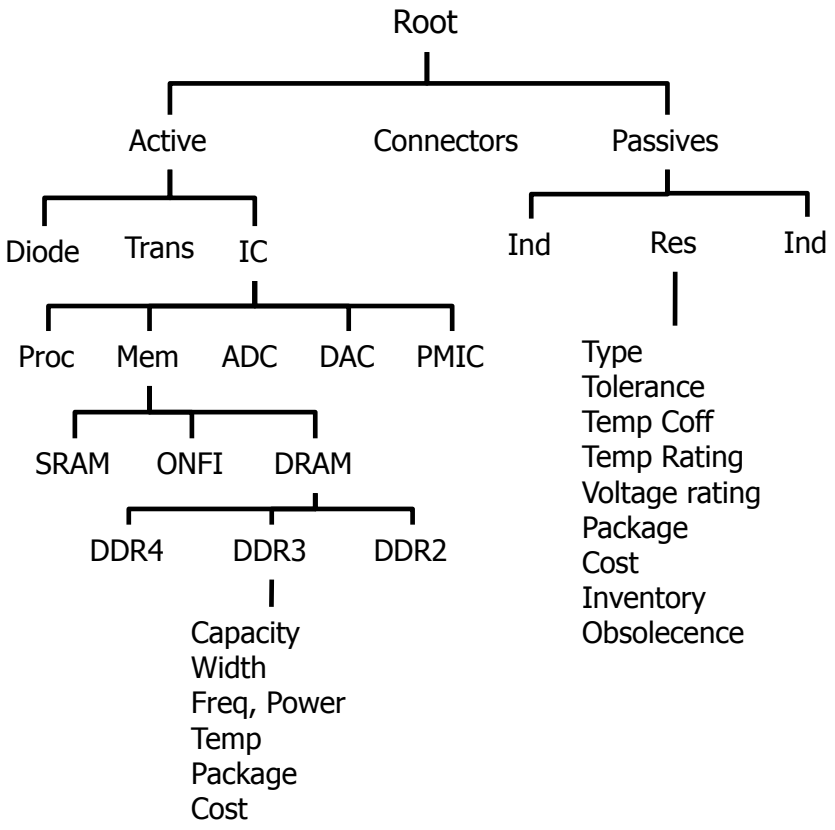
Today



Source: data sheets from Xilinx, Analog Devices

- 5M+ parts in circulation
- Information embedded in datasheets and reference designs
- No standard models
- Automatic optimization not possible

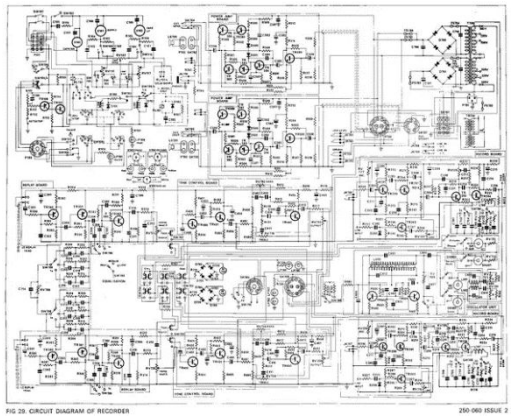
IDEA



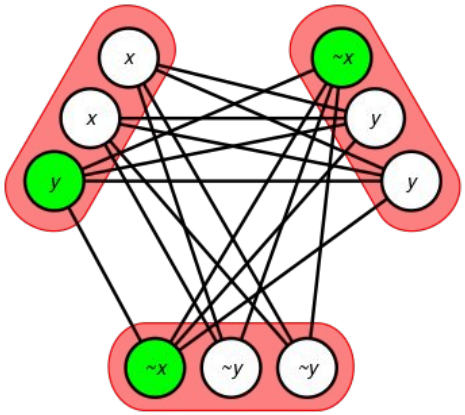
- IC standard models (LEF,LIB,IP-XACT)
- Extend standards for boards / SIPs
- Creation of 5M+ part DB
- Model all properties needed for constraint-based system optimization

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POSH: Expected Program Results



Open source analog IP



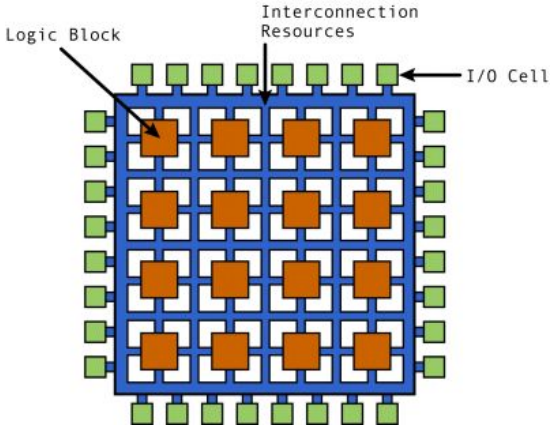
Signoff level validation



Commercial open source design community

RISC-V

Multicore RISC-V



Open source FPGA Chips



"Linux for SoC Design"

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Silicon Compiler Program Schedule

```
$ git clone https://github.com/darpa/idea
$ git clone https://github.com/darpa/posh
$ cd posh
$ make soc42
```



2018
- Program Kickoff

2018
- First Integration Exercise

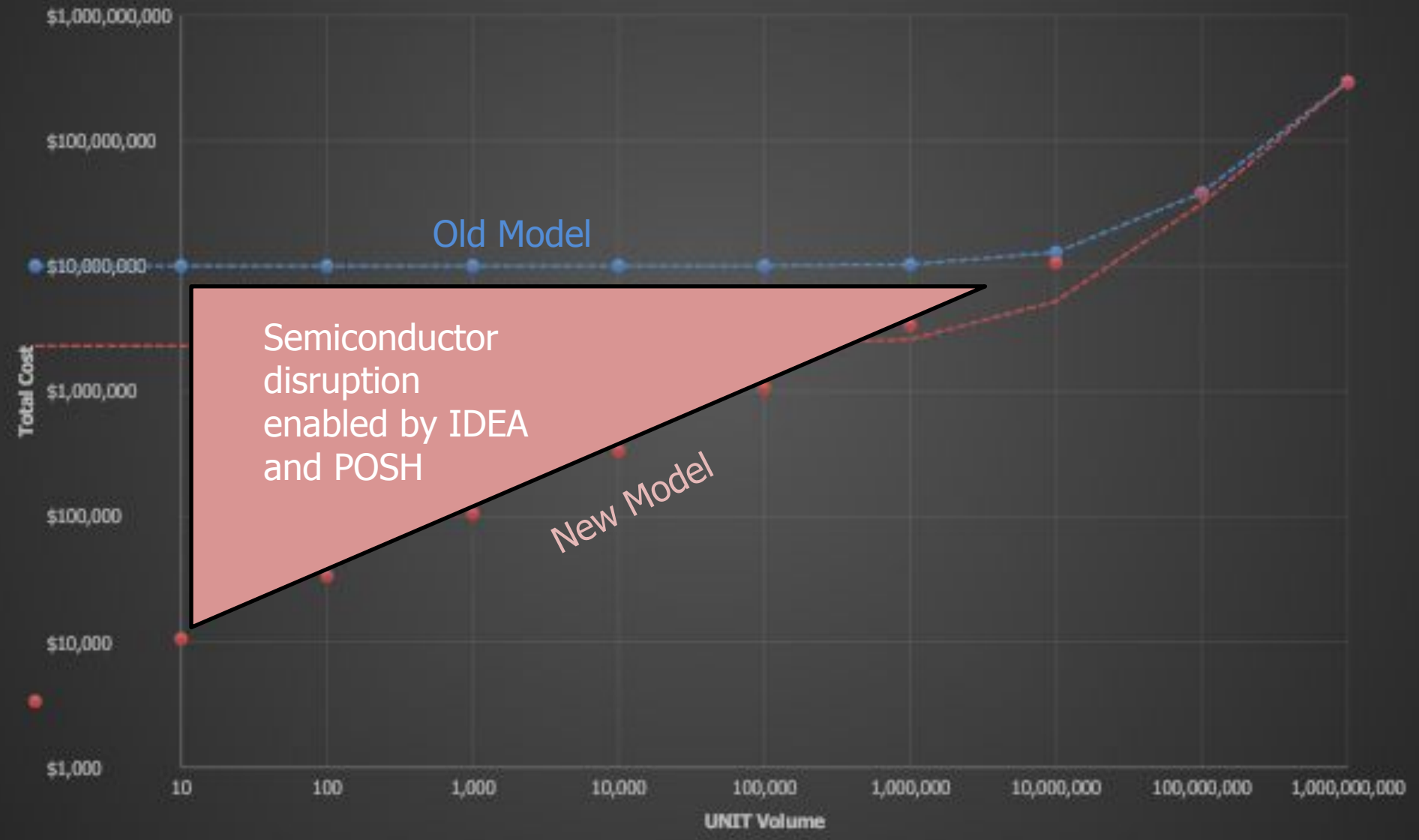
2019
- Alpha Release, working code

2020
- Working Beta Silicon Compiler
- 50% PPA

2022
- Program Completion
- 100% PPA

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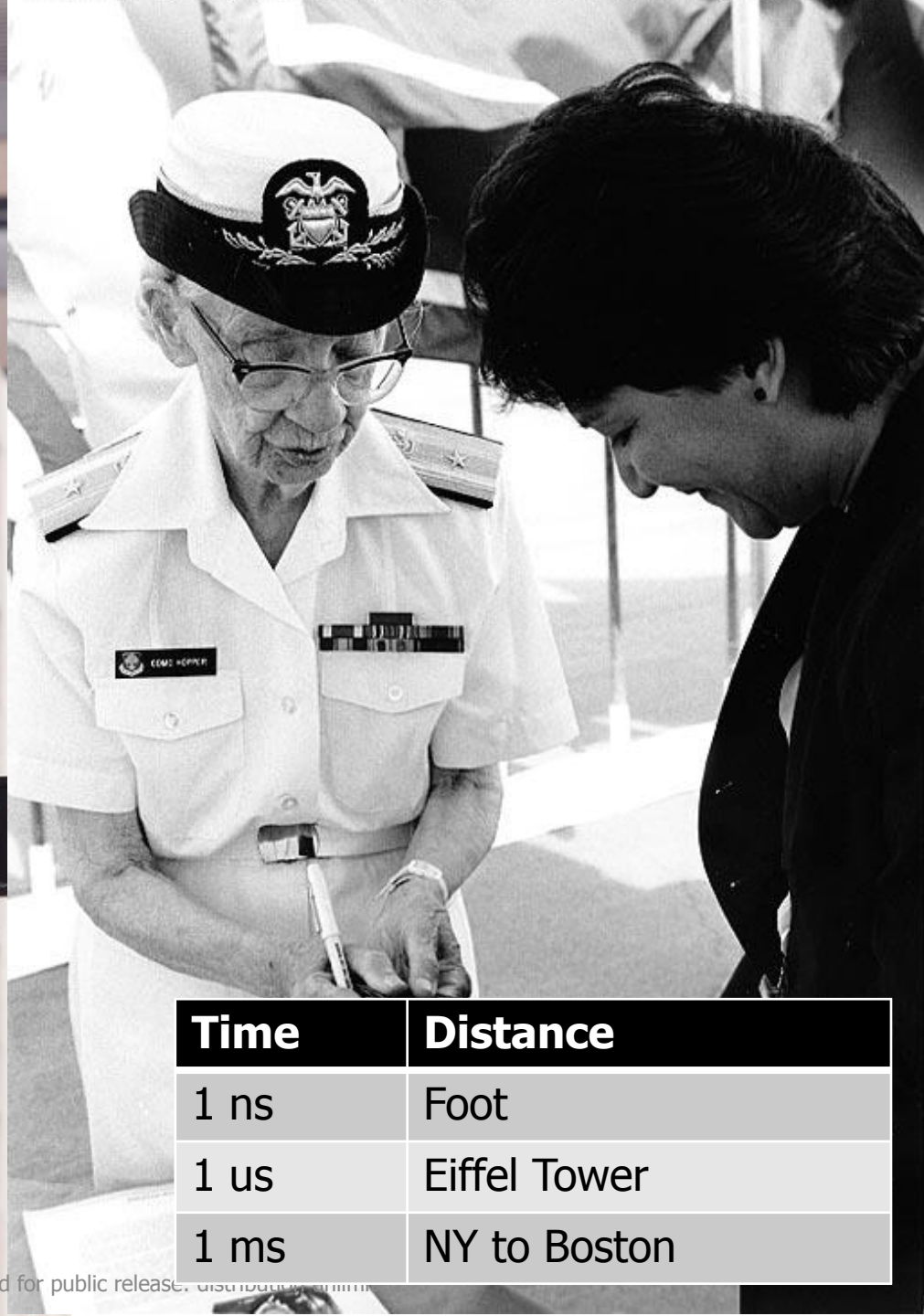
Money



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Time





Time	Distance
1 ns	Foot
1 us	Eiffel Tower
1 ms	NY to Boston

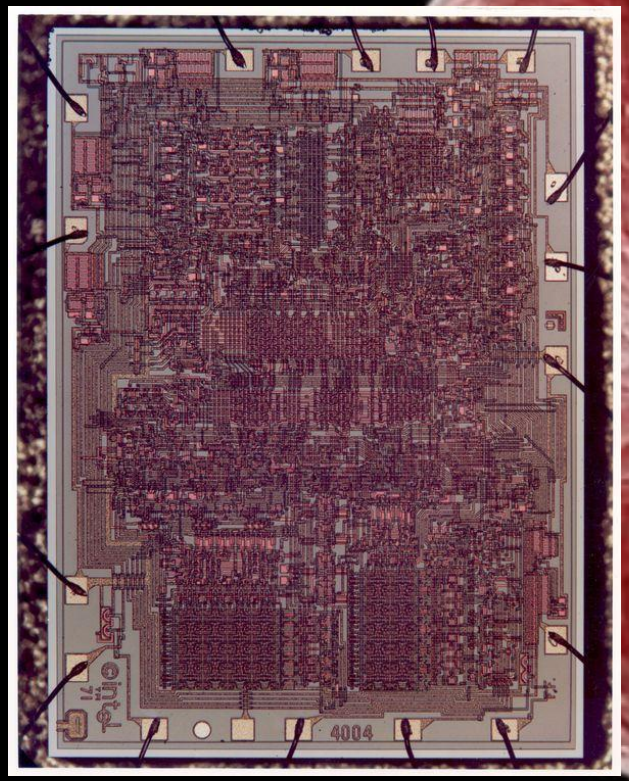
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Gravity



Real time machine learning?

Space



- Original Intel 4004
- 2,300 transistors
- Fits in a cell at 3nm

8um

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