Zero ASIC

Removing the barrier to custom silicon

Enabling Bespoke “N=1” Silicon

DAC 2023

Presented by Andreas Olofsson
andreas@zeroasic.com

Zero ASIC Overview

Business model	Design and sell custom System-In-Package devices
Founded	2008 (Adapteva), relaunched as Zero ASIC in 2020
Headquarters	Cambridge, MA
Employees	18
Average Experience/Employee	13 years
Funding	Government Contracts



My path to enlightenment→position statement

1996: VLSI course, “drawing” 4-bit ALU in Virtuoso

1998: ADI, Intro to logic synthesis (beat full custom CMOS design!)

1999-2006: ADI, Detour into custom logic (domino, self timed, transfer gates…)

2006-2008: ADI, **a**gile mixed signal codesign (>100M units shipped)

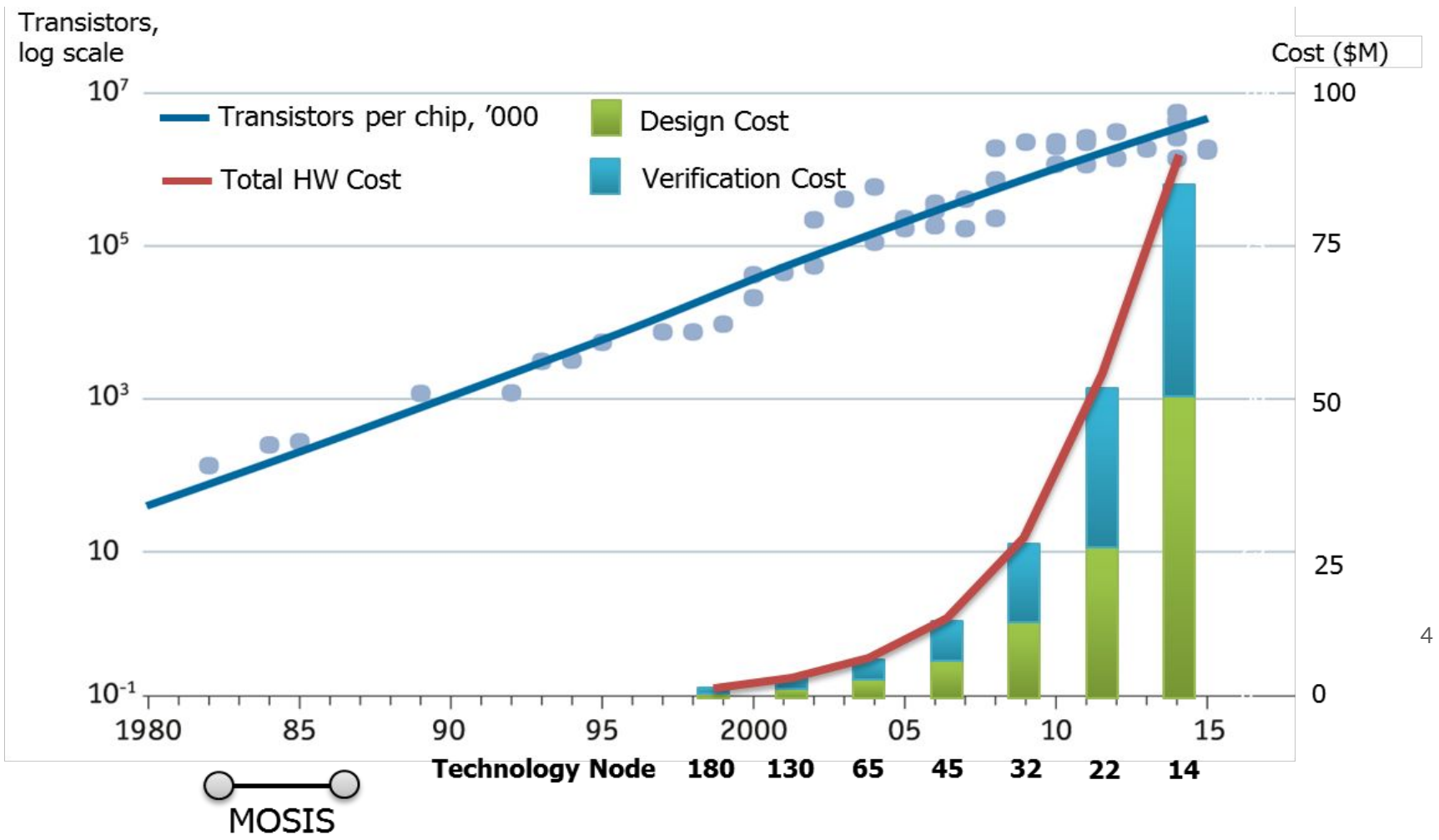
2008-2016: Adapteva**,** double down on codesign (4.5B transistors in 24 hours at 16nm)

2017-2019: DARPA, build technology to enable N=1 silicon. (N is the # units shipped)

2020-2023: ZeroASIC, built-to-order silicon systems based on pre-fabbed chiplets.

CHIPLETS (IF DONE RIGHT) WILL CHANGE THE INDUSTRY AND THE WORLD!!

Thesis: Chiplets is the only path to reduce design cost by by 100X!



Chiplets is the next natural evolution in IP reuse!

(removes mask costs, integration, sw, verification, eda, qual…)

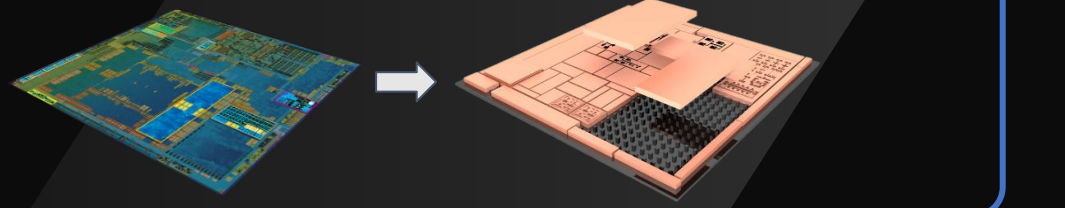
DARPA CHIPS Program (2016-2021)

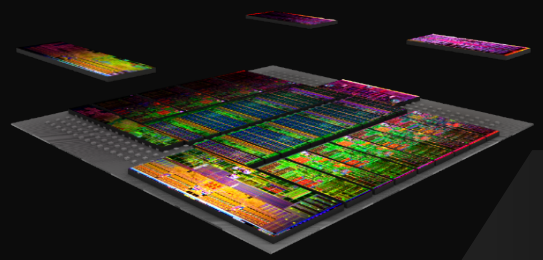
CHIPS Goals:

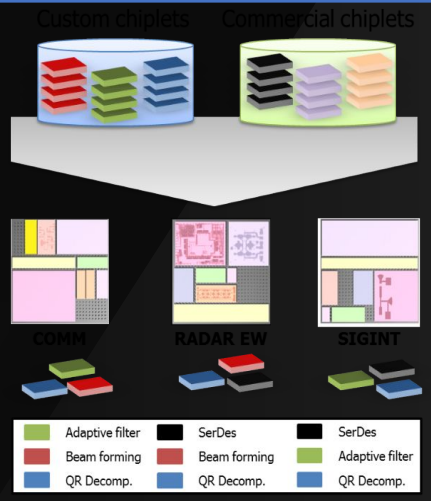
- ✔ A universal efficient interface standard
- ✔ SOTA manufacturing assembly
- ✔ A large and critical set of IP chiplets

Today: Monolithic

Tomorrow: Heterogeneous









Extend Moore's law
Scale out and scale down while managing yield

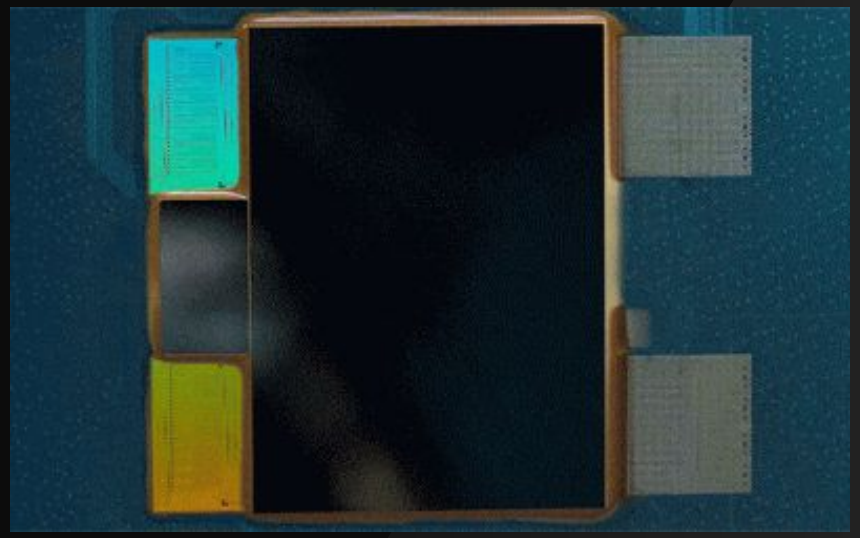
Enable heterogeneous integration
Materials/processes, companies, geography, security

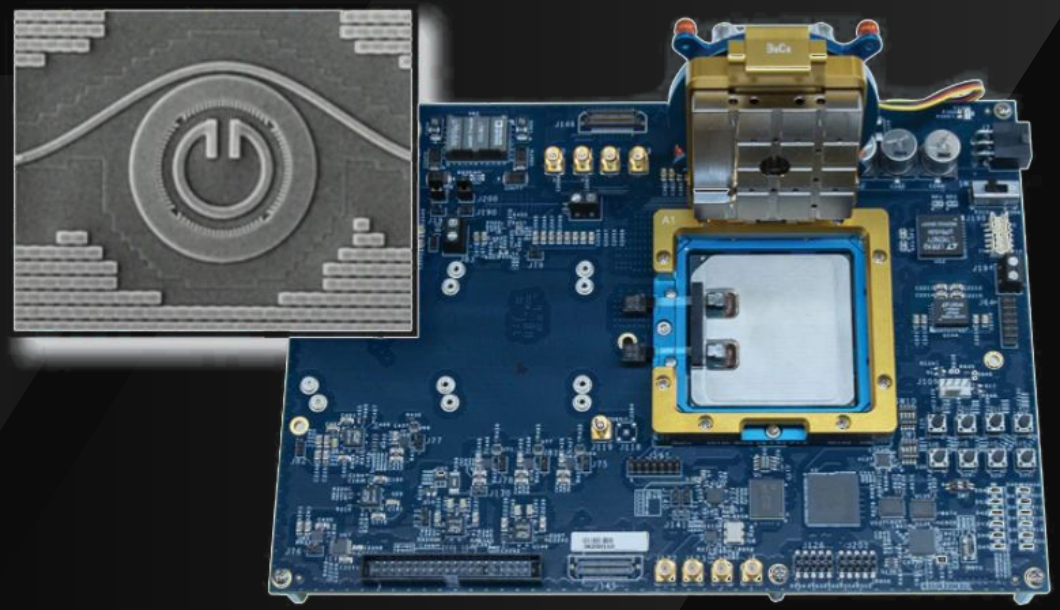
Empower system integrators
Democratize access to leading edge silicon for system integrators

zero

DARPA CHIPS Success #1: HI Integration (Terabit Optical Transceiver Integration)

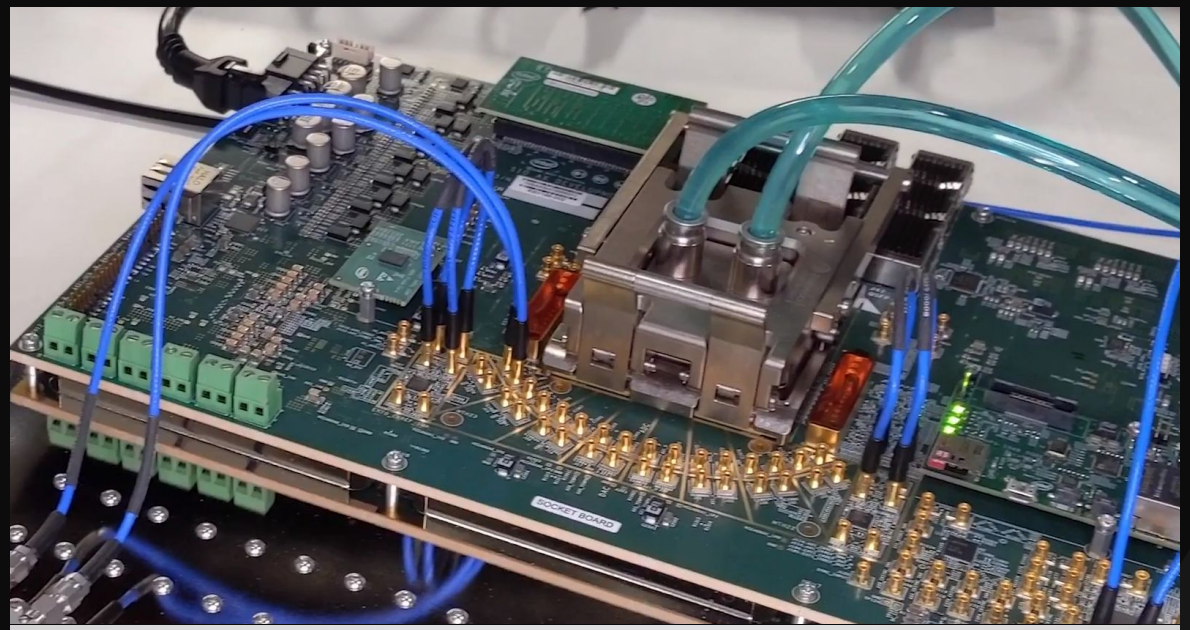


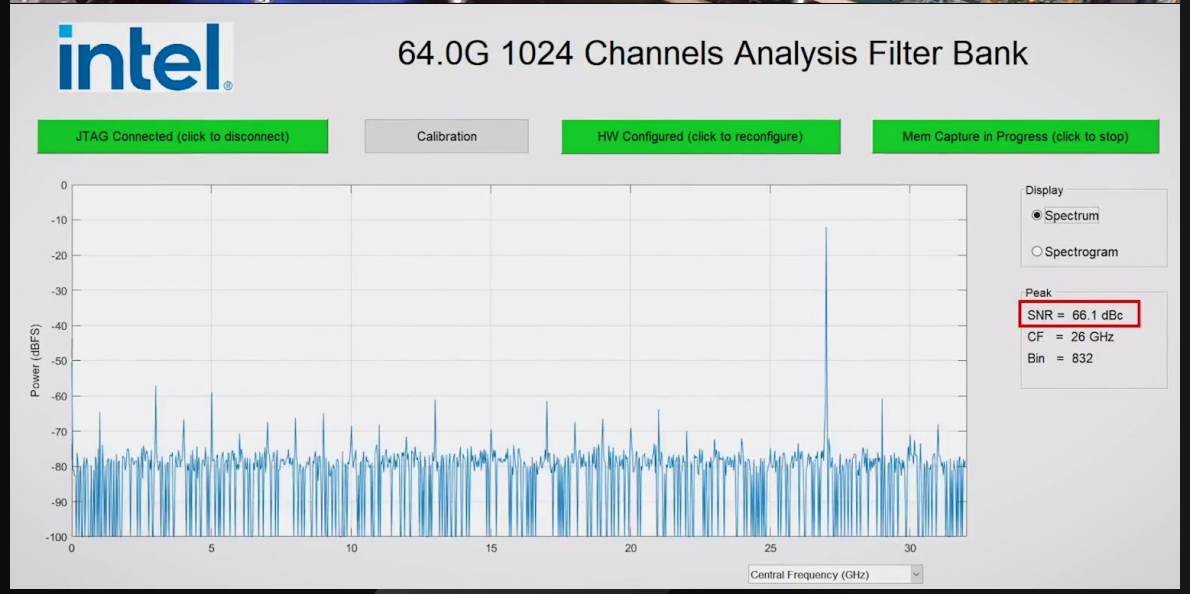


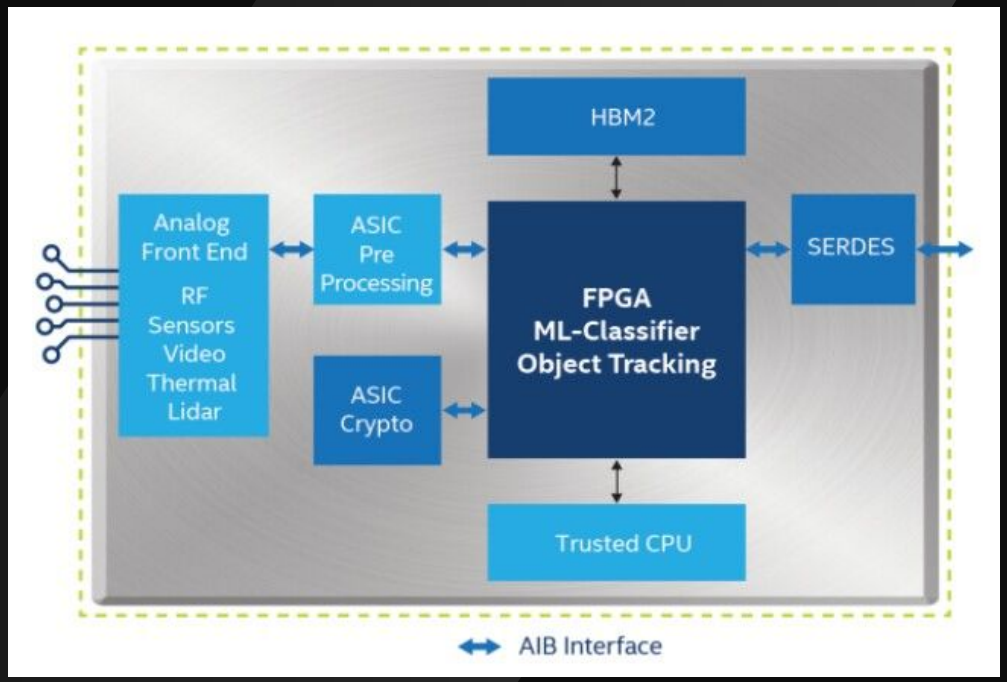


	Value
Bandwidth	960Gbps
Height	8.86mm
Width	5.5mm
Latency	10ns
Reach	2km
Efficiency	<5pJ/bit

DARPA CHIPS Success #2: A Chiplet Ecosystem (AIB based)







- 8 external silicon partners
- 4+ technology nodes
- 3 FPGA families
- 3 data converter chiplets
- 2 ASIC compete chiplets
- 9 serdes/optical IO chiplets

REMAINING GRAND CHALLENGES

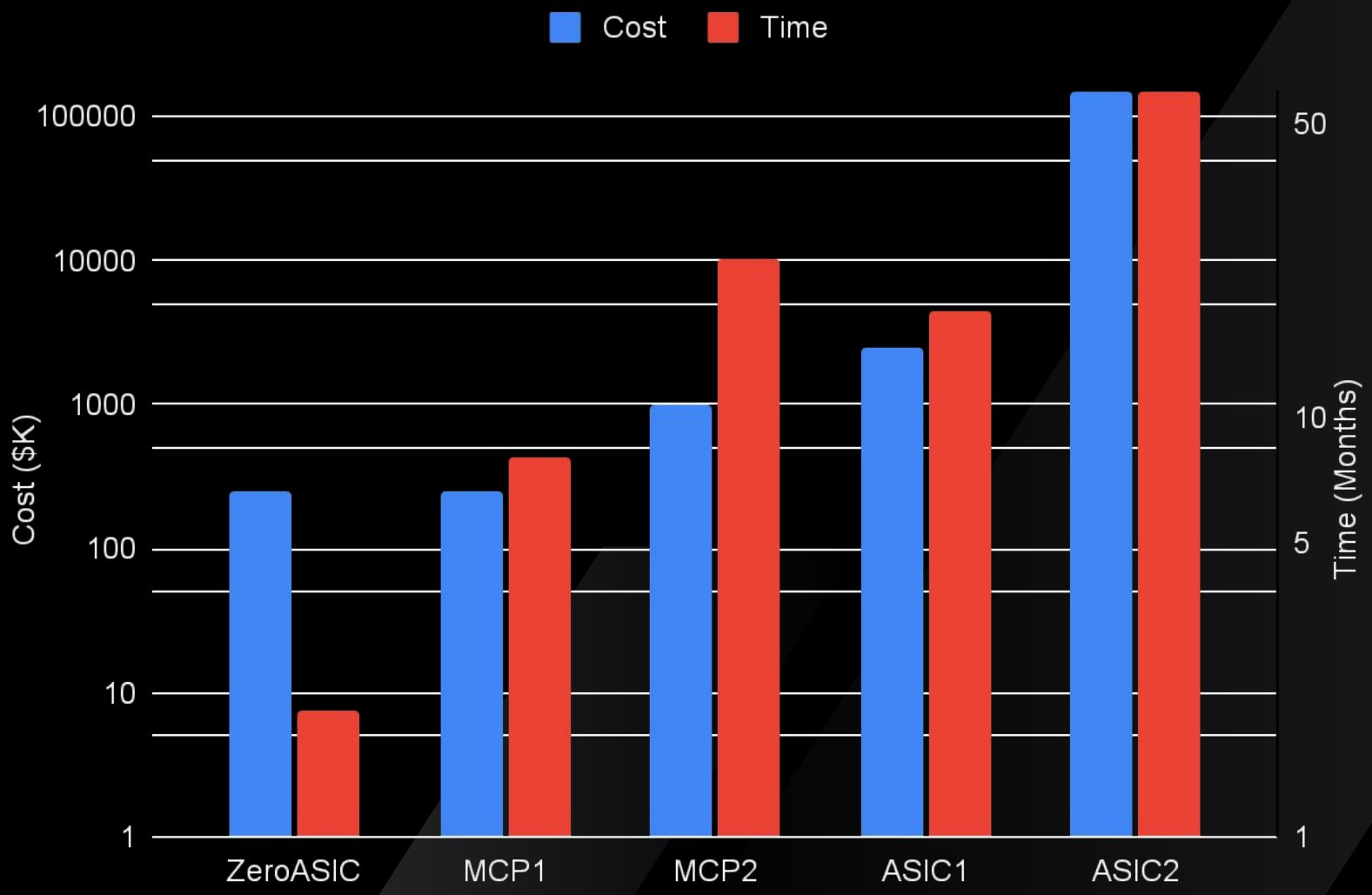
- Incomplete standards →need “ethernet/ddr for chiplets”
- Manufacturing not ready for N=1 model (or N<1,000,000…)
- Assembly must be separate from foundry to enable HI
- Every new product involve at least one tapout (what’s the point?)
- Chiplet based design costs is way to high (>>1$M)
- Chiplet design timeline too long (>1year)

Standards Challenge

	Electrical	Product	Protocol	Bidir	Footprint	3D	Speed/pin (Gbps)	Energy (pJ/bit)	Latency (ns)
AIB 1.0	Yes	Yes	No	Yes	No	No	2	1	<2
UCIE	Yes 1.0	No	Yes	Yes	No	No	32	0.5	<2
BOW	Yes	No	No	Yes	No	No	16	0.5	<5
HBM3	Yes	Yes	Yes	No	Yes	No	6.4	1	>100

- No full stack standard exists…even after 6 years…sad!
- No 3D standard
- No clear path to a chiplet ecosystem (KGD) business model

Cost Challenge: Reduce access barrier to advanced MCPs



NOTES:

ZeroASIC: NRE cost per project

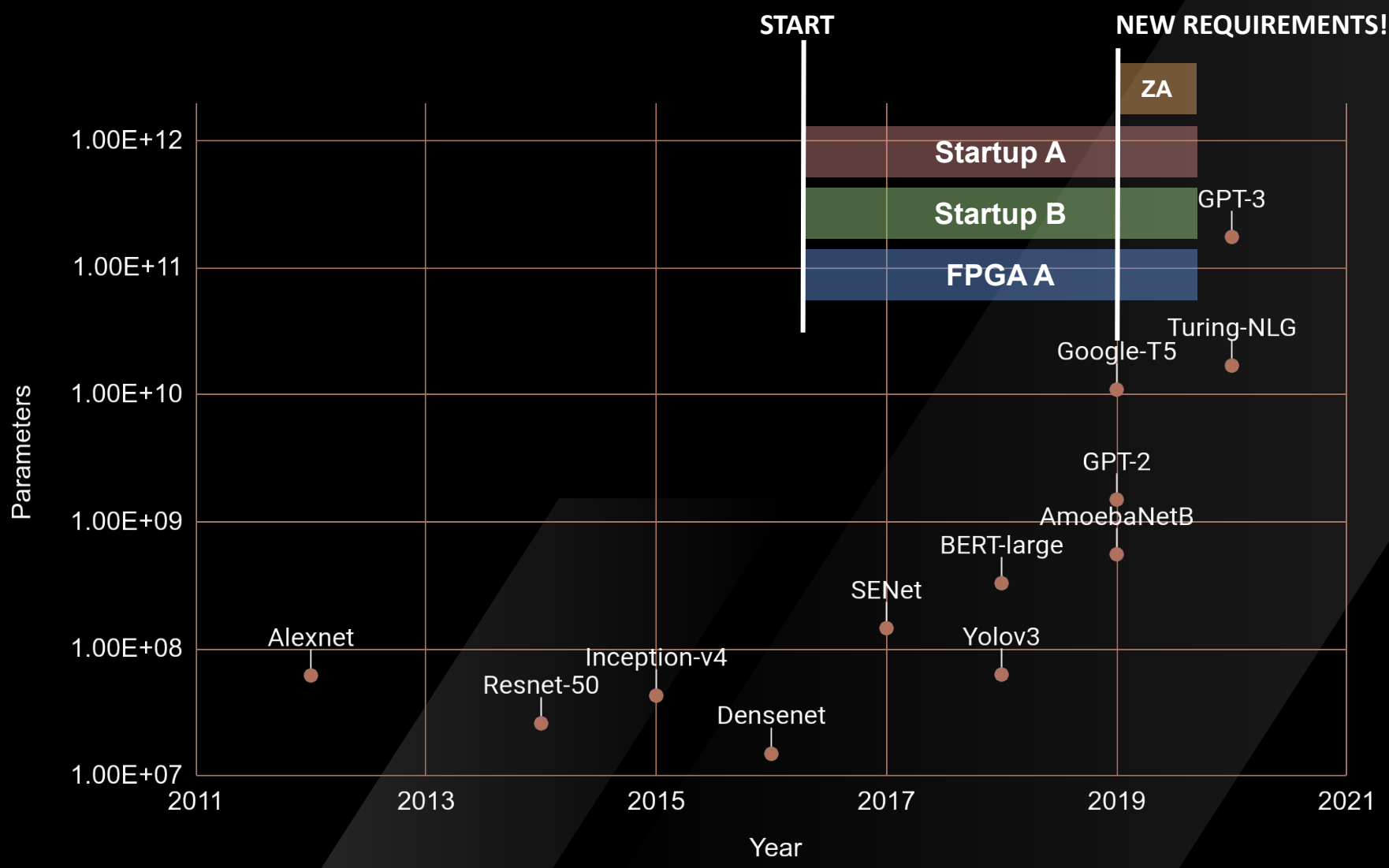
MCP1: Simple non-risk MCM at commercial pricing.

MCP2: Complex single source advanced packaging MCM.

ASIC1: Typical DoD ASIC.

ASIC2: Complex DoD SoC.

Time Challenge: $10B ASICs being designed for yesterday's AI!



The Problem:

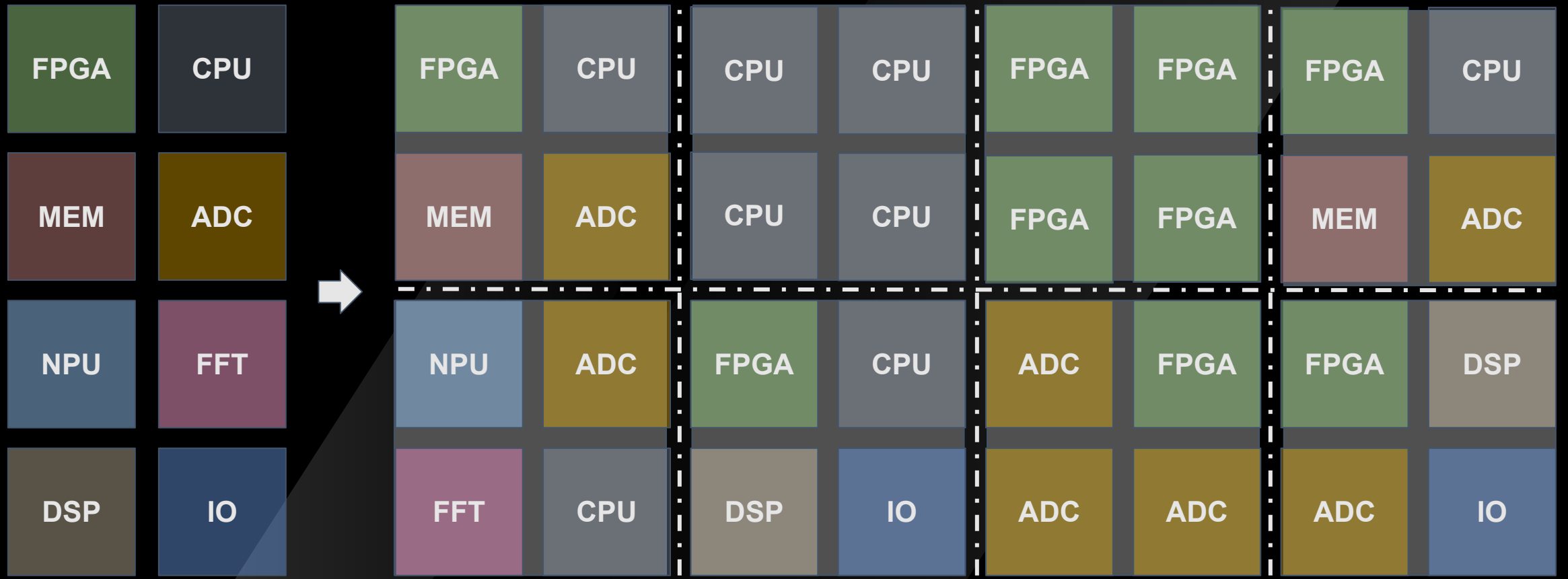
AI market moves so fast that domain specific chips are already obsolete when they hit the market

The Solution:

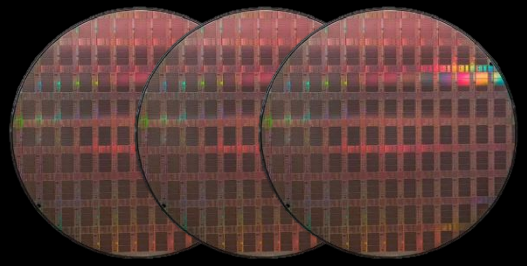
Zero ASIC offers chiplet programmability and late System-In-Package hardening of memory, compute, and IO mix.

Composability Challenge: Billions of unique systems from a small set of chiplets

Product Variations	n=library size, k=efabric sockets	Products (n=32, k=16)	Products (n=8, k =16)
Combinations (unordered)	n!/k!(n-k)!	1e8	–
Permutations (no repetition)	n!/(n-k)!	1e22	–
Permutations (repetition)	n^k	1e24	2e14

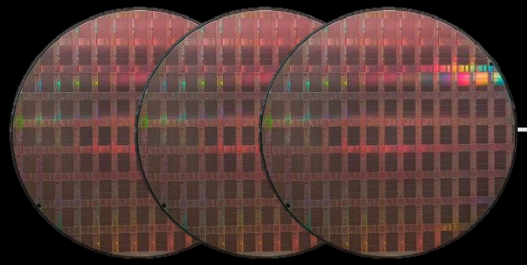


N=1 System Vision: Standardization + Inventory + Automation + APIs



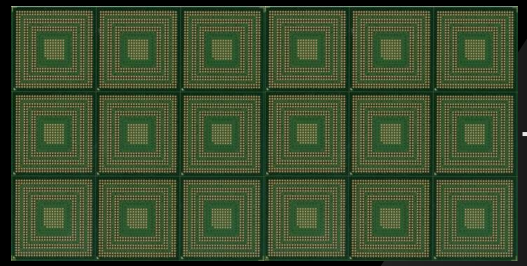
API

Chiplet Inventory



API

Interposer Inventory

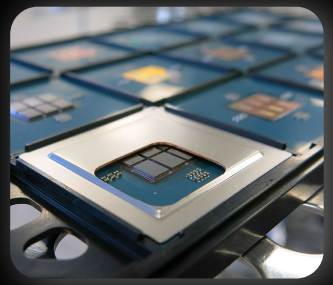


API

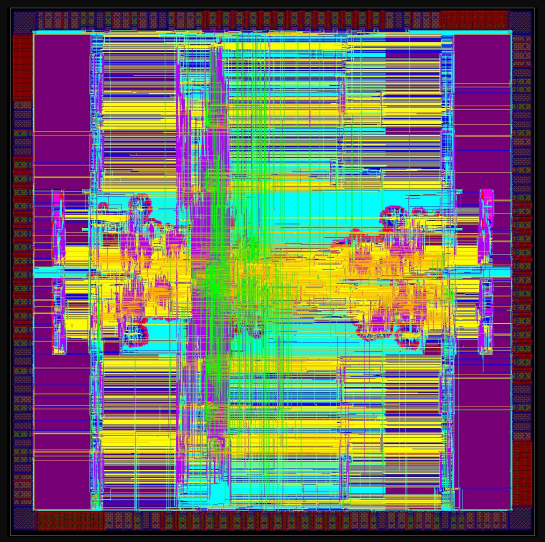
Substrate Inventory

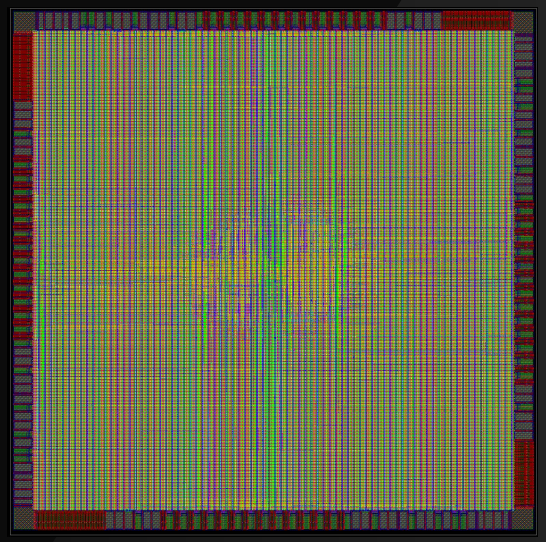
AUTOMATED MANUFACTURING PIPELINE

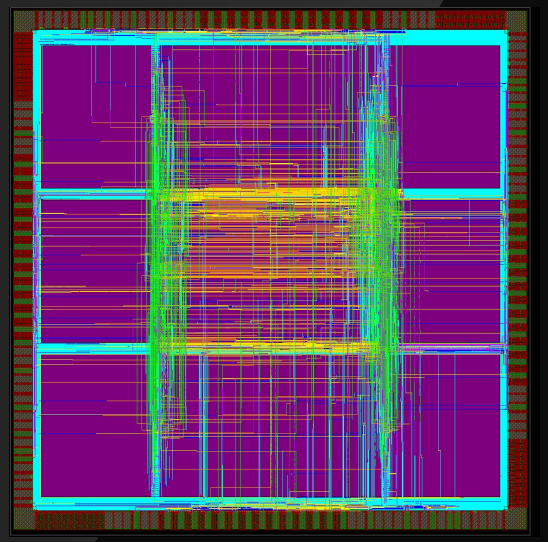




Zero ASIC Chiplet Status







	GOTLAND	MAUI	KODIAK
TYPE	CPU	FPGA	MEMORY
SIZE	2 x 2 mm	2 x 2 mm	2 x 2 mm
ORIGIN	UCB - ROCKET	ZA	ZA
METRIC	Quad Core RV64GC CPU	–	3MB
DESIGNERS	2	2	2
WALL TIME	< 8 weeks	< 8 weeks	< 8 weeks
RUN TIME	< 24hrs	< 24hrs	< 24hrs

Thank you!